Fig. 1

Fig. 2a

Fig. 2

SCAN / SENSOR

ENCODER

RAM

I / O PORT

TRANSCIEVER

DATA BUFFER

PROCESSOR

ADMINISTRATION INTERRUPT

Fig. 3

DOOR 1

DOOR 2

DOOR 3

L1

L2

L3

30a

Fig. 4

DISPLAY &
KEYBOARD

62

61

PROCESSOR
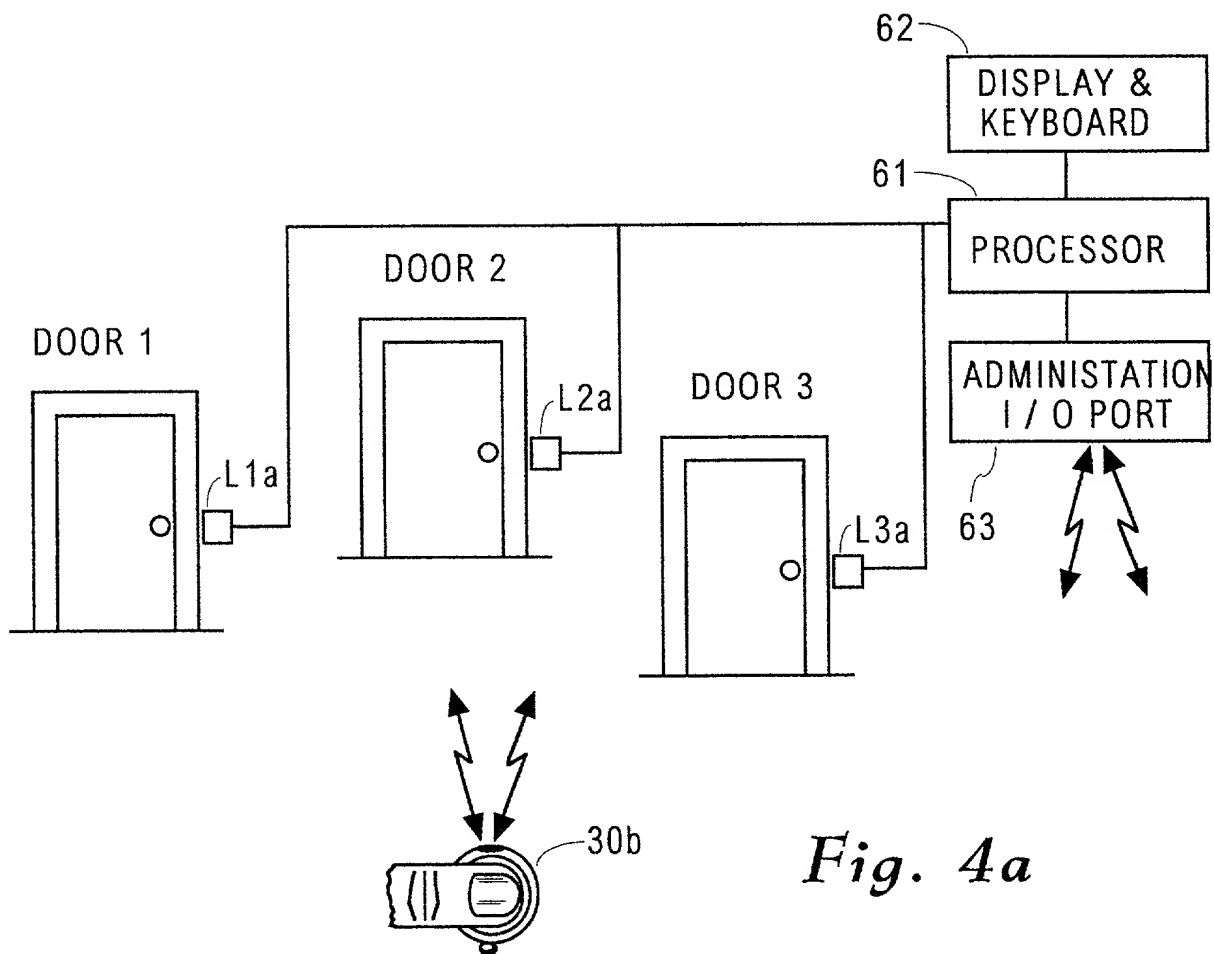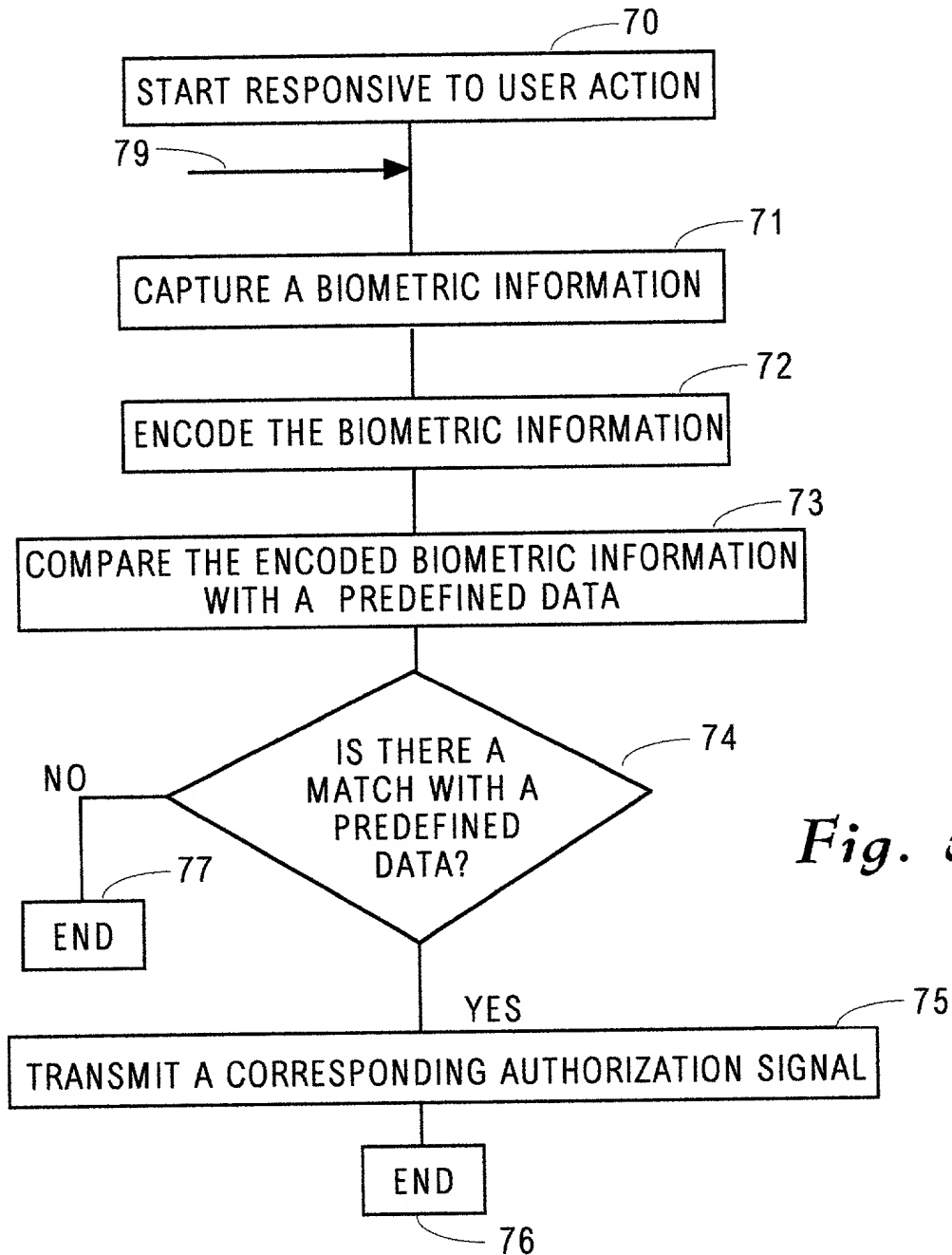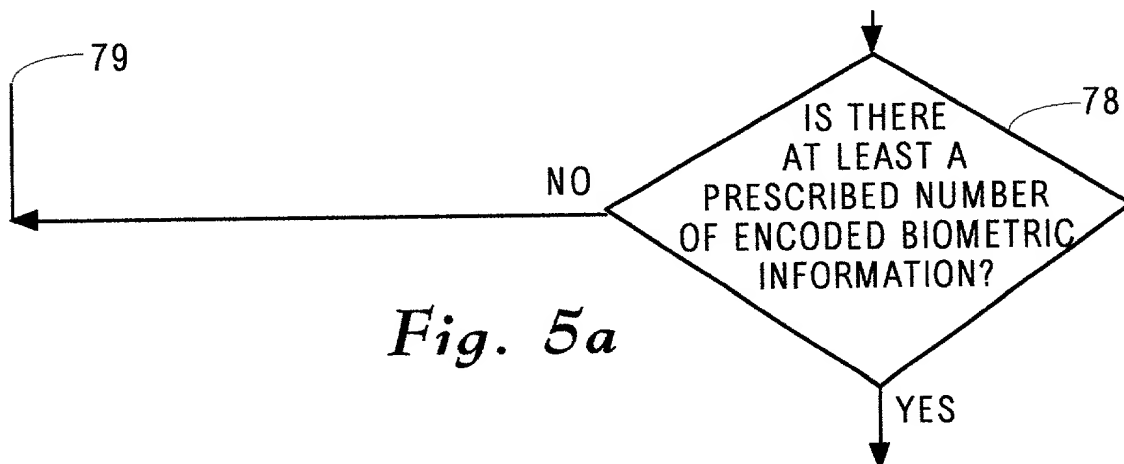
DOOR 2
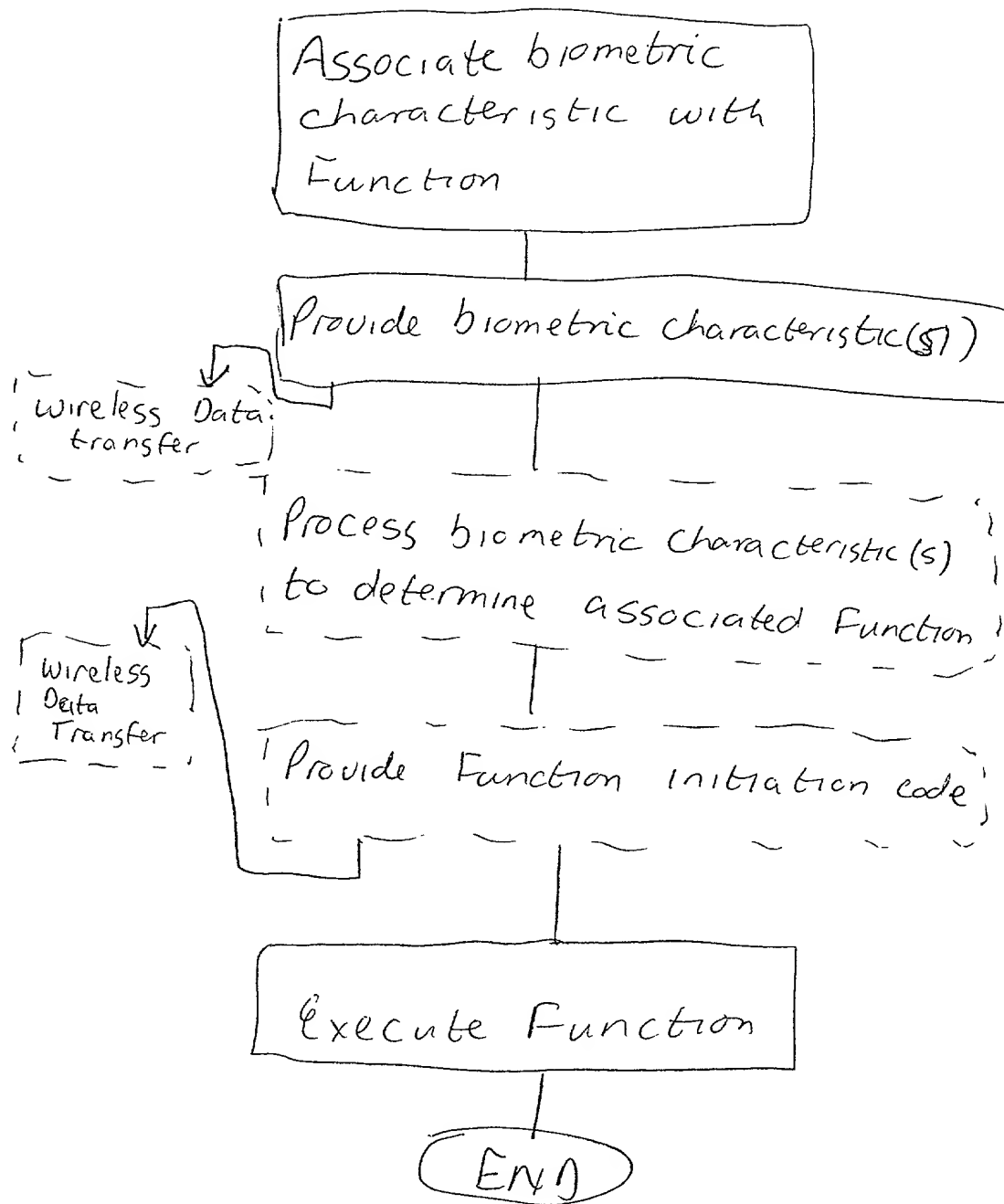
DOOR 1

DOOR 3

ADMINISTRATION
I / O PORT

L1a

L2a

L3a

63

30b

Fig. 4a

Fig. 5

Fig. 5a

Fig. 6